REMARKS

This Amendment is filed in response to the Office Action dated January 13, 2005. For the following reasons this amendment should be entered, the application allowed, and the case passed to issue. No new matter or considerations are introduced by this amendment. The amendment to claim 13 is supported by originally filed claim 15.

Claims 1-13 and 16-18 are pending in this application. Claims 1-12 have been withdrawn pursuant to a restriction requirement. Claims 13 and 15-18 have been rejected. Claim 13 has been amended and claim 15 canceled in this response.

Claim Rejections Under 35 U.S.C. § 102

Claims 13 and 16-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Hayashi (JP 6-318561).

Claims 13 and 15-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by Minato et al. (U.S. PG-Pub 2003/0132450).

These rejections are traversed, and reconsideration and withdrawal thereof respectfully requested. The following is a comparison between the invention as claimed and the cited prior art.

An aspect of the invention, per claim 1, is a method of manufacturing an integrated semiconductor device having a plurality of semiconductor elements formed in a semiconductor layer. Each semiconductor element has a source of a first-conductivity-type semiconductor, a drain of the first-conductivity-type semiconductor and a body region of a second-conductivity-type semiconductor between said source and said drain. The method comprises the steps of implanting impurities concurrently into at least a predetermined part of the drain of one

semiconductor element and into a predetermined part of the drain of another semiconductor element. An implantation mask is used that includes a portion corresponding to the drain of the one semiconductor element and has a first opening ratio as well as a portion corresponding to the drain of the another semiconductor element and has a second opening ratio different from the first opening ratio. The one semiconductor element has a breakdown voltage higher than that of the another semiconductor element. The implantation mask used has the first opening ratio smaller than the second opening ratio. The one semiconductor element is adjacent to the another semiconductor element. A wall-shaped element-isolation insulating film for isolating the one semiconductor element from the another semiconductor element is provided in the semiconductor layer prior to the step of implanting impurities. The integrated semiconductor device is annealed after the step of implanting impurities to diffuse the impurities.

The Examiner asserted that Hayashi (Figs. 1-4) discloses a method of manufacturing an integrated semiconductor device formed in a semiconductor layer having sources and drains, and implanting impurities through an implantation mask having different opening ratios (A, A'). The Examiner further asserted that Hayashi discloses that the semiconductor elements have different breakdown voltages, and that the masks illustrated in Fig. 4 include stripe-shaped masks and masks with dot-like openings. The Examiner maintained it is inherent, absent evidence to the contrary, that the mask having the smaller opening ratio is used for fabricating the semiconductor element of a higher breakdown voltage.

The Examiner averred that Minato (para. [0113] and Figs. 100-116) discloses a method of manufacturing an integrated semiconductor device formed in a semiconductor layer having sources 6 and drains 3, and implanting impurities through an implantation mask 41 having different opening ratios (para. [0112] and claim 36). The Examiner further averred that Minato

discloses that the semiconductor elements have different breakdown voltages, and that the masks include stripe-shaped masks (para. [0396] and [0404]). The Examiner concluded that claims 17 and 18 do not further limit the method.

Hayashi does not anticipate the claimed method of manufacturing an integrated semiconductor device because Hayashi does not disclose the step of providing the wall shaped-shaped element-isolation insulating film. The Examiner implicitly acknowledged that Hayashi does not disclose this feature, as claim 15 was not rejected in view of Hayashi.

Minato does not anticipate the claimed method of manufacturing an integrated semiconductor device because the Minato does not **identically** disclose a single method comprising all the claimed steps. Minato discloses many different embodiments of manufacturing a semiconductor device. The Examiner picks and chooses among the many different embodiments to reconstruct the claimed method using hindsight. "[R]ejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in "the prior art."" Thus, the reference must clearly and unequivocally disclose the claimed invention "without any need for picking, choosing, and combining various disclosures not directly related to each other by the teachings of the cited reference." *In re Arkley*, 455 F.2d 586, 587, 172 USPQ 524 (C.C.P.A. 1972).

Furthermore, Minato does not disclose the step of providing the wall-shaped element isolation insulating film for isolating semiconductor elements from each other. In addition, the object of the Minato invention is to improve the withstand (breakdown) voltage of one transistor, while an object of the present invention, which includes a plurality of transistors, is to simultaneously improve the on resistance and breakdown voltage of each of the transistors.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the disclosure in a single reference of each element of a claimed invention. *Helifix Ltd. v. Blok-Lok Ltd.*, 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994); *Hoover Group, Inc. v. Custom Metalcraft, Inc.*, 66 F.3d 399, 36 USPQ2d 1101 (Fed. Cir. 1995); *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051 (Fed. Cir. 1987). Because Hayashi and Minato do not disclose the step of providing the wall-shaped element-isolation insulating film for isolating the one semiconductor element from the another semiconductor element, prior to the step of implanting impurities, as required by claim 13, Hayashi and Minato do not anticipate claim 13.

Applicants further submit Hayashi and Minato, whether taken alone, or in combination do not suggest the claimed method of manufacturing an integrated semiconductor device.

The dependent claims are allowable for at least the same reasons as claim 13 and further distinguish the claimed invention. The Examiner's conclusion that claims 17 and 18 do not further limit the method is incorrect. Claim 17 further requires that the implantation mask used is a mesh implantation mask having dot-like openings dispersed in a masking portion. Claim 18 further requires that the implantation mask being used is a dot implantation mask having dot-like masking portions dispersed in an opening. Clearly, claims 17 and 18 further limit and distinguish the claimed method. The Examiner has provided no basis for asserting that the claims 17 and 18 do not further limit the method. The Examiner's conclusory statement that claims 17 and 18 "fail to further the limit the method making but only its device structure" is

unsupported. Claims are to be considered as a whole. The Examiner is not free to ignore claim limitations.

In view of the above remarks, Applicants submit that this amendment should be entered, the application allowed and the case passed to issue. If there are any questions regarding these remarks or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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